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APPLICANT: Subhash C. Roy et al.

SERIAL NO.: 09/918,123 GROUP ART UNIT: 21

FILED:July 30, 2001 EXAMINER:

FOR:Real Time Debugger for Embedded Systems ATT'Y DOCKET:TRA-040C1

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

I hereby certify that this correspondence is being deposited on this day with the United States Postal Service as first class mail in an envelope addressed to : Commissioner of Patents and Trademarks, Wasington, D.C. 20231.

David P Gordon Nov. 13, 2001

David P. Gordon Date
Reg. No. 29,996

Sir:

SUBMITTAL OF DOCUMENTS PURSUANT TO DUTY OF DISCLOSURE

Pursuant to applicant's duty of disclosure under 37 CFR Section 1.56, enclosed is a completed form PTO-1449 as well as copies of the cited documents which relate to the above-referenced patent application. Since this document submittal is being presented prior to the first examination on the merits, no fee is due herewith.

US Patent No. 5,428,618 to Ueki et al. discloses a debugger apparatus and method having an event history recording capability.

US Patent No. 5,440,700 to Kaneko discloses a microprocessor including device for detecting predetermined instruction and generating bus cycle.

US Patent No. 5,473,754 to Folwell et al. discloses a branch decision encoding scheme.

US Patent No. 5,491,793 to Somasundaram et al. discloses a debug support in a processor chip.

US Patent No. 5,513,346 to Satagopan et al. discloses an error condition detector for handling interrupt in integrated circuits having multiple processors.

US Patent No. 5,544,311 to Harenberg et al. discloses an on-chip debug port.

US Patent No. 5,572,672 to Dewitt et al. discloses a method and apparatus for monitoring data processing system resources in real-time.

US Patent No, 5,640,542 to Whitsel et al. discloses an on-chip in-circuit-emulator memory mapping and breakpoint register modules.

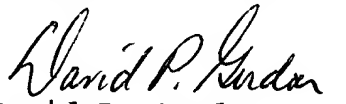
US Patent No. 5,724,505 to Argade et al. discloses an apparatus and method for real-time program monitoring via a serial interface.

US Patent No. 6,052,774 to Segars et al. discloses an apparatus and method for identifying exception routines indicated by instruction address issued with an instruction fetch command.

Motorola MPC860 User's Manual discloses a development system interface, Section 18, pages 20 thru 32.

The listed documents are brought to the Examiner's attention because they are known to the applicant and/or the applicant's attorney and may be considered by the Examiner to be material to his/her examination. This listing should not be construed as representation that a search has been made or that no better art exists. No inference should be made that the documents are in fact material merely because they are referenced herein. Moreover, no representation is made that the brief descriptions of the references herein necessarily describe the most material aspects of the references. Further, by this listing, the applicant is not making any admission regarding the relative dates of the invention and listed disclosures.

Respectfully submitted,



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